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## REMARKS/ARGUMENTS

Pending claims 1, 6-7,12, 19, 24, 26, 28, 33, 36, 38, and 44-45 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,488,709 (Chan). Applicant respectfully traverses the rejection and respectfully requests reconsideration of the same. As to claim 1, Chan nowhere teaches a substantial portion of the subject matter of claim 1. Specifically, Chan fails to teach: (1) determining in a processor if an update occurs to a data in a register; (2) a register of a processor; and (3) refraining from transferring register contents based on an indicator bit.

Chan nowhere teaches determining in a processor whether data of a register of a processor has been updated. Instead, all that Chan teaches is that when a memory stores data into a register, a valid bit is set. There is no determination made in a processor; instead, all the cited portions of Chan teach is that a memory update register 116 of a memory is loaded with data from a miss. That is, Chan is directed to a cache memory (i.e., cache memory 72) that includes a RAM array section 100, address latches and multiplexer section 102 and control logic 104. Chan, col. 7, lns. 10-20. Note that the memory update registers 116, contended by the Office Action to be processor registers, are present within the RAM array section 100 of this cache memory. Chan, FIG. 8B. As such, Chan fails to teach either a determination made in a processor, nor even the presence of a register of a processor. Clearly, Chan nowhere teaches determining in a processor whether data in a first portion of a register of the processor has been updated. As further support for the recited determining, the Office Action refers to setting of a valid bit within the memory update register 116, referring to column 33 of Chan. However, all that Chan teaches in this regard is that register 116 is used as a holding register for incoming data, and as data is returned by the system it is latched into one of the registers.

Furthermore, the system of Chan does not necessarily refrain from transferring the register contents (of register 116) to RAM array 100 based on the valid bit. In this regard, note the table on column 33 of Chan. As shown in that table, even when a set valid bit exists, data is not necessarily written from the register to RAM array 100 (see the last entry of the table). For all these reasons, the rejection of claims 1 and 7 is overcome.

As to dependent claims 6 and 44, the Office Action contends the teaching of a single indicator bit for multiple registers in Chan at col. 8, lns 25-28. However, all this portion of Chan teaches is that a line valid bit in a block directory entry associated with a cache line of a cache memory is set when the cache line is written. Such a cache line is not a register, nor is this bit

present within the cache line itself; instead it is in the block directory entry. Thus this bit is not in one of the recited plurality of registers. Accordingly, for these further reasons claims 6 and 44 are patentable.

Further still as to dependent claim 12, Chan does not teach that a single set indicator bit enables saving of the contents of multiple registers to a memory. Instead, as clearly taught in Chan (col. 33, lns. 45-68), "each byte of memory update registers 116A-116B is written to the RAM array section 100 if its valid bit is set ...." As such, not a single valid bit controls saving of the contents of multiple registers.

For similar reasons as to claim 1, independent claim 19 is also patentable. That is, Chan does not teach a processor having a register. This is so, as register 116, contended by the Office Action to be a processor register, is not, and instead is part of the cache memory of Chan. Claim 19 is patentable for the further reason that Chan nowhere teaches or suggests a context change, and Chan certainly nowhere discusses not transferring contents of a processor register to a memory on a context change if an indicator bit is not set.

As to dependent claims 26 and 33, the Office Action contends that memory update registers 116, which are indicated to be holding registers, are somehow control registers. Both of these dependent claims further recite that this control register is of a processor. In fact, the memory update register 116 of Chan is neither a control register nor is it of a processor. For these further reasons these dependent claims are patentable. Dependent claims 36 and 38 are also patentable for this further reason.

Dependent claim 45 is further patentable as Chan nowhere teaches not transferring contents of multiple registers if a single indicator bit has not been updated. As described above, Chan nowhere teaches a single valid bit for multiple registers. For this further reason, claim 45 is patentable.

The rejection of claims 34 and 37 under §103(a) over Chan in view of U.S. Patent No. 6,751,737 (Russell) is overcome at least for the same reasons as the independent claims from which these dependent claims depend. Furthermore, there is no motivation to combine the teaching of Chan which is directed to a memory, with the multiple protected mode execution environments of Russell. That is, as described above Chan nowhere deals with context switches. Nor is there any teaching or suggestion in either reference to combine their subject matter. Instead, the Office Action has clearly engaged in improper hindsight-based reconstruction to

combine the references. In order to prevent a hindsight-based obviousness analysis, the Federal Circuit requires that "to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant." *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1316-17 (Fed Cir. 2000). No such showing is present here.

As to the rejection of claims 35, 42, and 43 over §103(a) in view of Chan and Dynarski, the Office Action has again engaged in improper hindsight-based reconstruction. Nowhere does either reference teach or suggest reducing power consumption of a battery-operated device by refraining from transferring register contents. Nor is there any basis to combine the cache memory of Chan with Dynarski, which is directed a network access server. Thus this rejection also suffers from a hindsight-based reconstruction.

Pending claims 1, 7 and 19 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 6,012,135 (Leedom). Applicant respectfully traverses the rejection. As to claim 1, Leedom does not teach determining in a processor whether data in a first portion of a processor register has been updated. In this regard, the Office Action refers to an activity register 810 in Leedom. While this register does include a valid bit, this valid bit is to indicate that the register is valid for an outstanding activity. There is no determination as to whether data in a first portion of the register has been updated. Instead, this activity register is associated with writing data into a separate cache memory, i.e., a cache line 610. Because the cache line and activity register are separate, there can be no determination of whether data in a first portion of the register of a processor has been updated. Further, there is no setting of an indicator bit if data in that first portion is updated. Instead, the valid bit is set when a different register indicates that 16 words of data have been returned to a cache line 610. Because each of these entities, namely activity register 810, counter register 812, and cache line 610 are separate, the rejection of claim 1 is overcome.

Nor does Leedom anywhere teach refraining from transferring the register contents back to a memory based on the indicator bit. That is, the activity register 810 of Leedom is nowhere taught to be sent back to a memory. Instead, all that this register does is to aid in controlling completion of a given activity. Leedom, col. 14, lns. 55-58. However, Leedom nowhere teaches that any part of activity register 810 is sent to a memory, and it is certainly not done so based on

the valid bit. Accordingly, claim 1 is patentable over Leedom. For at least the same reasons claims 7 and 19 are similarly patentable.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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